



Docket No.: 57454-138

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Yasuhiko TSUKIKAWA

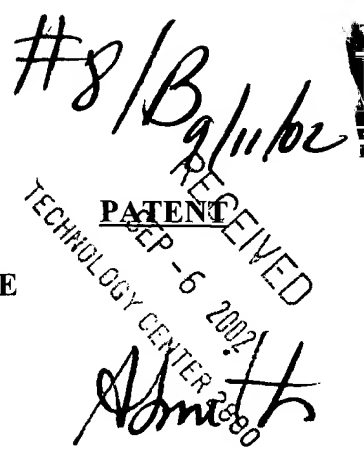
Serial No.: 09/877,027

Filed: June 11, 2001

For: CONFIGURATION FOR GENERATING A CLOCK INCLUDING A DELAY
CIRCUIT AND METHOD THEREOF

Group Art Unit: 2811

Examiner: Linh M. NGUYEN



AMENDMENT UNDER 37 C.F.R. 1.111

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

The following amendment and remarks are submitted in response to the Official
Action mailed June 5, 2002. Please amend the application as follows.

IN THE CLAIMS

Please amend claims 1, 4, 11 and 14 as follows:

1. (Amended) A delay locked loop comprising:

a delay circuit delaying a first clock to output a second clock;

a detector detecting which of said first and second clocks is advanced in a phase;

and

a gray code counter using a gray code, responsive to an output of said detector for
generating a signal to increase or decrease an amount of delay of said delay circuit.

B1 C1